

**WHAT IS CLAIMED IS:**

1. A method for use in connection with an integrated circuit design, the method comprising:

selecting a subset of low threshold voltage variants of gate instances for substitution with respective standard threshold voltage variants thereof.
2. The method of claim 1, wherein the selecting is based at least in part on a measurement indicating a substantial low threshold voltage variant timing penalty.
3. The method of claim 2, wherein the measurement includes an input slew rate of each gate instance in a circuit path.
4. The method of claim 3, wherein the input slew rate is based at least in part on falling edge input transitions.
5. The method of claim 2, wherein the measurement includes a delay for a low threshold voltage variant that is greater than the delay for a corresponding standard threshold voltage variant.
6. The method of claim 2, wherein the measurement includes a first maximum delay timing path calculation for a circuit path.
7. The method of claim 6, wherein the first maximum delay timing path calculation is based at least in part on a path cycle time for each circuit path including a low threshold voltage variant.
8. The method of claim 6, wherein the measurement includes a second maximum delay timing path calculation for a circuit path.
9. The method of claim 8, wherein the second maximum delay timing path calculation is based at least in part on a path cycle time for each circuit path including a standard threshold voltage variant corresponding to the low threshold voltage variant.

10. The method of claim 8, wherein the measurement includes the difference between the first and second maximum delay timing path calculation.
11. The method of claim 2, wherein the timing penalty exceeds a threshold.
12. The method of claim 1, further comprising substituting in the integrated circuit design, the selected low threshold voltage variants with the respective standard threshold voltage variants thereof.
13. The method of claim 12, further comprising fabricating an integrated circuit including the substituted standard threshold voltage gate instances.
14. The method of claim 1, further comprising preparing the integrated circuit design and thereafter performing the selecting for substitution.
15. A semiconductor integrated circuit comprising:
  - a plurality of gate instances;
  - circuit paths defined through respective ones of the gate instances;
  - wherein a subset of the gate instances are standard threshold voltage variants substituted in the semiconductor integrated circuit based on a measurement indicating a low threshold voltage variant penalty for the circuit paths including the subset of the gate instances.
16. The semiconductor integrated circuit of claim 15, wherein the measurement includes input slew rates for gate instances in the circuit paths including the subset of the gate instances.
17. The semiconductor integrated circuit of claim 16, wherein the input slew rate is based at least in part on falling edge input transitions.
18. A computer readable encoding of a semiconductor integrated circuit design, the computer readable encoding comprising:
  - one or more design file media encoding representations of a plurality of gate instances; and

one or more design file media encoding representations of circuit paths defined through respective ones of the gate instances, wherein a subset of the gate instances are standard threshold voltage variants substituted in the semiconductor integrated circuit based on a measurement indicating a low threshold voltage variant timing penalty.

19. The computer readable encoding of a semiconductor integrated circuit design of claim 18, wherein the measurement includes input slew rates for gate instances in the circuit paths including the subset of the gate instances.

20. A method of making a computer readable media product that encodes a design file representation of a semiconductor integrated circuit, the method comprising:

preparing the one or more design files for the semiconductor integrated circuit including at least one low threshold voltage instance and performing timing analysis thereon;

substituting at least one of the low threshold voltage instances of the semiconductor integrated circuit with a standard threshold voltage instance; and

generating one or more design file outputs that encode representations of the semiconductor integrated circuit, including the substituted standard threshold voltage instances; and

supplying the one or more design file outputs as at least part of the computer readable media product.

21. The method of making a computer readable media product that encodes a design file representation of a semiconductor integrated circuit of claim 20, wherein the substituting is based at least in part on a measurement indicating a low threshold voltage variant timing penalty.

22. The method of making a computer readable media product that encodes a design file representation of a semiconductor integrated circuit of claim 20, wherein the substituting is based at least in part on a measurement including input slew rates for gate instances in the circuit paths including the subset of the gate instances.

23. An apparatus comprising:

means for processing one or more design files for a semiconductor integrated circuit, the one or more design files encoding representations of a plurality of gate instances and circuit paths;

means for selecting at least one of the gate instances based on a measurement that indicates a low threshold voltage variant timing penalty; and

means for substituting at least one of the low threshold voltage gate instance representations with respective standard threshold voltage variants thereof.